Code :RR320504 RR

III B.Tech II Semester(RR) Supplementary Examinations, April/May 2011
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering, Computer Science & Systems Engineering, Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks
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1. Explain different parallel processing mechanisms that are possible in uniprocessor computers.
2. (a) Differentiate between Static and Dynamic Pipelines.
   (b) Compare and contrast Unifunctional and Multifunctional pipelines.
   (c) Explain the concept of Instructional pipeline.
3. (a) Explain the conceptual view of a single stage interconnection network and a switch.
   (b) Give basic organization of Illiac-IV array processor.Explain the its operation.
4. Discuss sorting patterns with respect to three ways of indexing the$PE's$.
5. (a) Explain how two K-maps are connected in a cross-cluster memory access of a loosely coupled Multiprocessor.
   (b) Differentiate between Homogeneous Multiprocessors and Heterogeneous Multiprocessors.
6. (a) What is meant by cache coherence? Explain how this problem can be avoided.
   (b) Derive an expression for processor utilization U, for the multiprocessor system with set-associative caches.
7. (a) Explain the organization of a static data flow computer.
   (b) What are the major design issues of a data flow computer? Explain in detail.
8. (a) Discuss about a simple queuing structure with a single processor having inter arrival time and service times.
   (b) Discuss in detail the performance of M/M/n queuing structure.

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